IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Andricacos et al

Docket No. YOR91995137X

Application No.:

Art Unit:

Filed:

Examiner:

For: Electroplated Interconnection Structures on Integrated Circuit Chips

PRELIMINARY AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INTRODUCTORY COMMENTS

Prior to examination, please amend the above-identified U.S. patent application as follows:

Amendments to the Specification begin on page 2 of this paper.

Remarks/Arguments begin on page 3 of this paper.